REMARKS

Claims 1-7, 15-26, and 30-32 are pending. Claims 30-32 have been added. Claims 1, 15, and 19 are in independent form.

In the action mailed April 4, 2005, claims 1-7 and 15-26 were rejected under 35 U.S.C. § 112, first paragraph as allegedly failing to contain a written description of the claimed subject matter. Also, the drawings were rejected under 37 C.F.R. § 1.83(a) as not showing features recited in the claims.

Both of these issues are obviated by the present amendments to claims 1, 15, and 19. In particular, claims 1, 15, and 19 all relate to register sets that comprise a plurality of two-ported random access memory devices. *See, e.g.*, element 76b, FIG. 3 and page 22, line 28-29 (identifying banks A and B). The fact that each register set comprises two effective read ports and one effective write port is also apparent from element 76b of FIG. 3.

In light of these amendments, the rejections and objection are believed to be moot.

Claim 1 was rejected under 35 U.S.C. § 103(a) as obvious over U.S. Patent No. 5,933,627 to Parady (hereinafter "Parady").

As amended, claim 1 relates to an execution unit for execution of multiple context threads. The execution unit comprises an arithmetic logic unit to process data for executing

threads, control logic to control the operation of the arithmetic logic unit, and a general purpose register set to store and obtain operands for the arithmetic logic unit. The register set comprises a plurality of two-ported random access memory devices. The register set comprises two effective read ports and one effective write port. Each bank is capable of performing a read and a write to two different words during the same processor cycle.

Parady neither describes nor suggests such an execution unit. In particular, Parady neither describes nor suggests a register set that comprises a plurality of two-ported random access memory devices and two effective read ports and one effective write port.

The rejection of claim 1 contends that Parady's integer registers 48 constituted a register set constructed with a two-ported random access memory architecture. However, Paraday is silent as to the architecture of integer registers 48. Indeed, integer registers 48 appear to be standard registers with hardware ports as shown in FIG. 1. Hence, nothing about Parady's registers describes or suggests a plurality of two-ported random access memory devices. Even if integer registers 48 comprises two effective read ports and one effective write port, integer registers 48 is not a "general purpose register" set as claimed.

Thus, Parady neither describes nor suggests a register set that comprises a plurality of two-ported random access memory devices and two effective read ports and one effective write port. Accordingly, claim 1 and the claims dependent therefrom are not obvious over Paraday.

Claim 15 was rejected under 35 U.S.C. § 103(a) as obvious over Parady.

The rejection of former claim 15 contends that claim 15 is nearly identical in scope to claim 1. Applicant respectfully submits that claim 1 relates to an execution unit for the execution of multiple context threads, whereas claim 15 relates to a method for executing multiple context threads.

The method of claim 15 includes processing data for executing threads within an arithmetic logic unit, operating control logic to control the arithmetic logic unit, storing and obtaining operands for the arithmetic logic unit within a general purpose register set comprising a plurality of two-ported random access memory devices. The register set comprises two effective read ports and one effective write port. Each bank is capable of performing a read and a write to two different words in the same processor cycle.

Parady neither describes nor suggests such a method. In particular, Parady neither describes nor suggests storing and obtaining operands within a general purpose register set

comprising a plurality of two-ported random access memory devices.

Paraday is silent as to the construction of integer registers 48. Indeed, integer registers 48 appear to be standard registers with hardware ports as shown in FIG. 1, and hence do not describe or suggest a general purpose register set comprising a plurality of two-ported random access memory devices. Thus, even if integer registers 48 comprises two effective read ports and one effective write port, integer registers 48 is not a general purpose register set as claimed.

Thus, Parady neither describes nor suggests storing and obtaining operands within a general purpose register set comprising a plurality of two-ported random access memory devices and two effective read ports and one effective write port. Accordingly, claim 15 and the claims dependent therefrom are not obvious over Paraday.

Claim 19 was rejected under 35 U.S.C. § 103(a) as obvious over Parady.

As amended, claim 19 relates to a processor unit that includes an execution unit for execution of multiple context threads. The execution unit includes an arithmetic logic unit to process data for executing threads, control logic to control the operation of the arithmetic logic unit, and a general purpose register set to store and obtain operands for the

arithmetic logic unit. The register set comprises a plurality of two-ported random access memory devices. The register set comprises two effective read ports and one effective write port.

Parady neither describes nor suggests such a processor unit. In particular, Parady neither describes nor suggests a register set comprises a plurality of two-ported random access memory devices and two effective read ports and one effective write port.

The rejection of former claim 19 contends that Parady's integer registers 48 constituted a register set constructed with a two-ported random access memory architecture. However, Paraday is silent as to the architecture of integer registers 48. Indeed, integer registers 48 appear to be standard registers with hardware ports as shown in FIG. 1. Hence, Paraday's integer registers 48 neither describe nor suggest a a register set comprising two-ported random access memory devices. Even if integer registers 48 comprises two effective read ports and one effective write port, integer registers 48 is not a general purpose register set as claimed.

Accordingly, claim 19 and the claims dependent therefrom are not obvious over Paraday.

Applicant hereby petitions under 37 C.F.R. §1.136 for a two-month extension of time up to and including September 4, 2005. A check for $450 is enclosed. Please apply any charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

BY JOHN F. CONROY REG. NO. 45,485

Date: 8/29/05

Scott C. Harris
Reg. No. 32,030
Attorney for Intel Corporation

Fish & Richardson P.C.
PTO Customer Number: **20985**
12390 El Camino Real
San Diego, CA 92130
Telephone: (858) 678-5070
Facsimile: (858) 678-5099
10525740.doc